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DOCUMENT-IDENTIFIER: US 5956052 A
** See image for Certificate of Correction **
TITLE: Image forming apparatus with means for correcting image density
non-uniformity

Detailed Description Text (146):
In the foregoing embodiment, the apparatus functions as a copying machine, wherein
the image reading apparatus is connected with the ink jet recording apparatus, and
the density correcting process is executed in the image reading apparatus. However,
the present invention is not limited to this case, but is applicable to another
case, for example, in which an ink jet recording apparatus receives R, G, B signals
from color VTR apparatus or the like, or to a facsimile apparatus. In the latter
case, the .gamma. correcting circuit for correcting the above-described density
non-uniformity correction is provided in a signal processor circuit in the ink jet
recording apparatus.

Detailed Description Text (170):
The CPU 712 is connected to the shading correcting circuit 703, the logarithmic
converter 704, the color correcting circuit 705 and the density non-uniformity
correcting circuit 706, and sets various conditions therefor. Furthermore, the CPU
712 is connected to a ROM 713 storing an operating program or the like, and to a RAM
714 storing various conditions or the like, so as to control the execution of the
program. The RAM 714 is backed up by a battery 715, so that the data are retained
even if the power source is shut down. The CPU 712 is further connected with an IC
card interface 715 so as to read the data stored in the IC card 717 functioning as
the storing means. Each of the recording heads 800Y, 800M, 800C and 800K has a ROM
30Y, 30M, 30C or 30K storing the serial number. The serial numbers are read by the
CPU 712. The CPU 712 and the density non-uniformity correcting circuit 706
constitute the control means.

Detailed Description Text (200):
As shown in FIG. 45A, an original is set on an original supporting platen in the
manner that the nozzle arrangement detection B of the standard test pattern (50%
halftone) for the non-uniformity measurement is perpendicular to the direction A of
the line sensor arrangement. Then, it is scanned by a line sensor. When the
resolution power of the recording head 100 and the resolution power of the line
sensor are the same, the density data of a number of picture elements are obtained
by one sampling operation by the line sensor, the number corresponding to the number
of light receiving elements of the line sensor. When the resolution power of the
line sensor (CCD) is higher than that of the recording head, the density of the
recorded one picture element is calculated on the basis of the data provided by
plural light receiving elements.

Detailed Description Text (237):
The ink jet recording apparatus may be used as an output terminal of an information
processing apparatus such as a computer or the like, a copying apparatus combined
with an image reader or the like, or a facsimile machine having information sending
and receiving functions.

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DOCUMENT-IDENTIFIER: US 5668642 A
** See image for Certificate of Correction **
TITLE: Image data communication apparatus capable of receiving image data during power failure

Abstract Text (1):
A facsimile apparatus has a communication unit, a memory for storing image data, and a back-up power supply for supplying power to the memory at power stoppage. The apparatus includes a detector for detecting power stoppage, and a control circuit for causing the communication unit to perform reception when the power stoppage is detected by the detector, and for causing the memory to store image data received by the communication unit, wherein the back-up power supply supplies power to the communication unit.

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DOCUMENT-IDENTIFIER: US 5708820 A
TITLE: Network hibernation system for suspending and resuming operation of computer
system operable in network environment in event of power failure or period of
inactivity

Detailed Description Text (6):
FIG. 3 illustrates a power supply 3 for providing back-up power supply to the
network hibernation system as constructed according to the principles of the present
invention. The power supply 3 comprises an AC (alternating current) power supply 30;
a power switch 31; a linear converting rectifier 32 composed of a transformer (TF)
having a primary coil connected to two output terminals of the AC-power supply 30
and a secondary coil providing parallel output terminals via diodes (D31, D32) and
condensers (C31, C32); a battery 34 and a battery charger 33 connected in cascade to
the linear converting rectifier 32; a power supply state detector 36 connected to
the output terminal of the linear convening rectifier 32; a power supply switching
state detector 36 connected to the power switch 31 for determining whether the AC
power is normal; a DC (direct current) converting controller 37 connected to the
output terminals of the power supply detector 35 and the power supply switching
state detector 36, for generating the power supply interruption detection signal to
a system part 3C in response to an abrupt termination of the power supply; a DC/DC
converter 38 connected to the output terminals of the battery charger 33 and the DC
converting controller 37, for providing an output DC voltage to an output terminal
of the bridge rectifier 3A1 in the main power supply 3A through a diode; a main
power supply 3A having the bridge rectifier 3A1 and a power supply 3A2 serially
connected to an output terminal of the AC-power supply 30 through power switch 31,
for supplying a 5 volts and 12 volts of DC power at respective output terminals; and
an augmented slot interrupter 3B connected to the 5 volts and 12 volts of DC power
and coupled to receive the power interruption detection signal.

Detailed Description Text (21):
The interrupt vector table stores address data of specific commands to be processed
by the CPU 11 of the system controller 1. The monitor/OS processing region stores
data used by a monitor or Basic Input/Output Software (BIOS) for operating the
system. The operating system region stores software for memory management, I/O
device management, process management such as, for example, MS-DOS. The network
driver region processes an interface between the hardware network interface as shown
in FIG. 4 and the software network interface. The network hibernation module or the
network hibernation information may be included in the network driver. The network
hibernation module region stores the network hibernation module for implementing the
suspension process of FIG. 7 and resuming process of FIG. 10. The network
hibernation information region contains configuration data for the network interface
hardware in step S54 of FIG. 5, steps S73 of FIG. 7, and S13, S15, S16 of FIG. 10.
The network software region communicates with the LAN server for transmitting and
receiving files. The free region reserves loading space for user application
software. The hibernation module processing region memorizes data needed to resume
operation of the computer after suspension, and parameter values needed to invoke
the network hibernation module in case of power-off and booting as shown in FIGS. 8
and 11.

CLAIMS:

15. The network hibernation system of claim 12, further comprised of said power
supply comprising:

a power switch for enabling transmission of said main power supply from said main

power source;

a linear converting rectifier comprising a transformer having a primary coil connected to said main power and a secondary coil connected to first and second output terminals of said linear convening rectifier via a respective diode and capacitor;

a battery and a battery charger connected in cascade to the first output terminal of said linear converting rectifier;

a power supply detector connected to the second output terminal of said linear converting rectifier, for detecting said main power supply rectified by said linear converting rectifier;

a power supply state detector connected to the power switch, for detecting said main power supply transmitted through said power switch;

a converting controller coupled to receive output signals of said power supply detector and said power supply state detector, for defecting abrupt termination of said main power supply from said main power source to generate said ac-down signal providing back-up power to said computer system;

a back-up power source having a bridge rectifier connected between said main power source via said power switch, for providing first and second voltage signals;

a DC/DC converter connected to said battery charger and said direct current converting controller, for providing a DC converted signal to the bridge rectifier of said back-up power source; and

an augmented slot interrupter comprising a first transistor having a first electrode of a principal electrically conducting channel connected to receive said first voltage signal and a second electrode of said principal electrically conducting channel connected to an augmented slot, and a second transistor having a first electrode of a principal electrically conducting channel connected to a control electrode of said first transistor and connected to receive said second voltage signal and a second electrode of said principal electrically conducting channel connected to a potential terminal, and a control electrode connected to receive said ac-down signal.